APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,600	12/17/1999	ALEX I. EYDELBERG	INTL-0304-US	9073

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TIMOTHY N TROP
TROP PRUNER HU & MILES PC
8554 KATY FREEWAY
STE 100
HOUSTON, TX 77024

EXAMINER
HA, LEYNNA A

ART UNIT	PAPER NUMBER
2135	5

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/465,600	EYDELBERG, ALEX I.
	Examiner	Art Unit
	LEYNNA T. HA	2135

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-30* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 has been reexamined and rejected under 35 U.S.C. 102(e).

2. Examiners Response.

3. Conclusion - Final Rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. ***Claims 1-30 are rejected under 35 U.S.C. 102(e) as being unpatentable by Rakavy, Et. Al. (US 6,324,644).***

As per claim 1:

Rakavy, et al. discloses a method comprising:

selectively loading either a first module of the basic input/output system or a second module of the basic input/output system based on a system state that indicates a connection to a network; **[see col.6, lines 24-43]**

executing said first basic input/output system module; and

[see col.6, lines 47-60]

dynamically linking to said second basic input/output system module.

[see col.12, line 56 thru col.13, line 2 and col.15, lines 3-13]

As per claim 2:

Rakavy, et al. discloses a method of claim 1 further comprising:

storing said first module of a basic input/output system for a processor-based system on a first storage device prior to execution; **[see col.6, lines 45-56]**

storing said second module of the basic input/output system on a second storage device prior to execution; and **[see col.5, lines 47-51]**

enabling said second module to be executed conditionally depending on a state of said processor-based system. **[see col.7, lines 13-26 and col.8, lines 7-29]**

As per claim 3:

Rakavy, et al. teaches a method of claim 2 wherein storing said second module includes storing said second module in a storage associated with a network

server accessible to said processor-based system over a network. **[see FIGs.1 and 7]**

As per claim 4:

Rakavy, et al. teaches a method of claim 1 further including detecting said system state during the boot sequence. **[see col.8, lines 44-65]**

As per claim 5:

Rakavy, et al. teaches a method of claim 4 including detecting whether or not the system is connected to a network during the boot operation. **[see col.9, lines 23- 43]**

As per claim 6:

Rakavy, et al. teaches a method of claim 1 including dynamically linking to one of a plurality of modules, and exporting and offset to an entry point in one module to another module. **[see col.7, lines 25-33 and col.8, lines 1-6]**

As per claim 7:

Rakavy, et al. teaches a method of claim 6 including storing a secondary entry point in a module to locate a function within the module. **[see col. 8, lines 7-29]**

As per claim 8:

Rakavy, et al. teaches a method of claim 7 including developing a segment address for said second module at run time. **[see FIG.3A]**

As per claim 9:

Rakavy, et al. teaches a method of claim 8 including providing a descriptor table which indicates a segment address for said second module. **[see col.15, lines 26- 43]**

As per claim 10:

As rejected on the same rationale as applied in claim 1.

As per claim 11:

As rejected on the same rationale as applied in claim 2.

As per claim 12:

As rejected on the same rationale as applied in claim 3.

As per claim 13:

Rakavy, et al. teaches an article of claim 11 further storing instructions that cause a processor-based system to execute said second module conditionally depending on whether or not the processor-based system is coupled to a network. **[see col.9, lines 5-42]**

As per claim 14:

Rakavy, et al. teaches an article of claim 11 further storing instructions that cause a processor-based system to selectively access either a first module setting forth a first authentication protocol in a first storage device or a second module setting forth a second authentication protocol in a second storage device. **[see col.13, line 40 thru col.14, line 49]**

As per claim 15:

Rakavy, et al. teaches an article of claim 11 further storing instructions that cause a processor-based system to dynamically link said first and second modules. **[see col.12, line 56 thru col.13, line 2 and col.15, lines 3-13]**

As per claim 16:

As rejected on the same rationale as applied in claim 4.

As per claim 17:

As rejected on the same rationale as applied in claim 5.

As per claim 18:

As rejected on the same rationale as applied in claim 6.

As per claim 19:

As rejected on the same rationale as applied in claim 7.

As per claim 20:

As rejected on the same rationale as applied in claim 8.

As per claim 21:

As rejected on the same rationale as applied in claim 9.

As per claim 22:

Rakavy, et al. discloses a processor-based system comprising:

a processor; **[see col.5, lines 46-48]**

a first basic input/output system module executable by said processor; and **[see col.6, lines 24-63]**

a second basic input/output system module executable by said processor, said second module being dynamically linked **[see col.12, line 56 thru col.13, line 2 and col.15, lines 3-13]** to said first module after selectively loading either said first module of the basic input/output system or said second module of the basic input/output system based on a system state that indicates a connection to a network **[see col.6, lines 24-63]**.

As per claim 23:

Rakavy, et al. teaches a system of claim 22 including a detector that detects a system state to determine whether said processor executes said second module. **[see col.9, lines 2-42]**

As per claim 24:

Rakavy, et al. teaches a system of claim 22 including a first storage for said first module and a storage second module for said second module, said second storage being coupled to said processor-based system over a network. **[see FIGs.1 and 2]**

As per claim 25:

Rakavy, et al. teaches a system of claim 24 wherein said detector detects information about network access. **[see col.9, lines 2-42]**

As per claim 26:

Rakavy, et al. teaches a system of claim 25 wherein said first and second modules include different authentication protocols. **[see col.9, lines 43-62 and col.13, lines 26-63]**

As per claim 27:

Rakavy, et al. teaches a system of claim 26 wherein said processor executes said basic input/output system module on said second storage to implement a network authentication protocol. **[see col.13, lines 26-63]**

As per claim 28:

Rakavy, et al. teaches a method of claim 22 wherein said first module dynamically links to said second module, using an offset exported from said second module. **[see col.7, lines 11 thru col.8, lines 28]**

As per claim 29:

Rakavy, et al. teaches a method of claim 28 wherein said first module uses a secondary entry point to locate a function in said second module. **[see col.8, lines 5-28]**

As per claim 30:

Rakavy, et al. teaches a method of claim 22 wherein said processor provides a descriptor table which indicates a segment address for said second module. **[see col.15, lines 26- 43 and FIG.3B]**

Response to Amendment

5.   The Examiner has examined the amended claims and in light of the new grounds of rejection, the Examiner maintains the rejection. Rekavy discloses selectively loading the BIOS based on the system state by having the ability to detect and load the network BIOS initialization entry point to give control to the network BIOS and allows multitasking between the conventional BIOS and the network BIOS (see col.6, lines 36-41). Rekavy further discusses more elaborately on the selectively loading of the BIOS based on the system state that indicates a connection to a network on col.7 thru col.8. Loading and executing in the real and protected modes are just additional details of Rekavy's invention and in fact has nothing to do with Applicant's claimed language for claims 1-30. The cited rejections above meets claims 1-30 as taught by Rekavy. Therefore, this Office Action is a Final rejection.

Conclusion

6.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
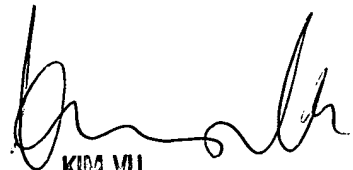
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEYNNA T. HA whose telephone number is (703) 305-3853. The examiner can normally be reached on Monday - Thursday (7:00 - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lha

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100